CLAIMS:

1. Tunable quadrature phase shifter comprising

- an input means (IN) for inputting an input signal (vin; iin),
- splitting means (10) for splitting the input signal into two essentially orthogonal first and second signals (i1, i2),
- adding means (6) for adding said first and second signals (i1, i2),
- subtracting means (7) for subtracting said first and second signals (i1, i2),
- a first output (OUT+) for outputting a first output signal (vo1) based on the output signal from said adding means (6), and
- a second output (OUT-) for outputting a second output signal (vo2) based on the output signal from said subtracting means (7),

characterized in that said splitting means (10) is provided as an all-pass.

2. Phase shifter in accordance with claim 1,
characterized by a first output buffer means (14) for buffering said first output signal (vo1), and a second output buffer means (15) for buffering said second output signal (vo2).

3. Phase shifter in accordance with claim 1 or 2,
characterized by a first transimpedance converter (12) having its input connected to said input means (IN).

4. Phase shifter in accordance with at least any one of claims 1 to 3,
characterized by

- a second transimpedance converter (14) having its output connected to said first output (OUT+), and
- a third transimpedance converter (15) having its output connected to said second output (OUT).

5. Phase shifter in accordance with claim 3 and/or 4,
characterized in that the transimpedance converter (12; 14; 15) is a transimpedance amplifier.

6. Phase shifter in accordance with claims 2 and 4, characterized in that said first and second output buffer means are said second and third transimpedance converters (14, 15), respectively.

7. Phase shifter in accordance with at least any one of claims 1 to 6, characterized by at least

- a first transistor (T_1) with its collector connected to its base and its emitter coupled to a predetermined potential,
- second transistor (T_2) with its base connected to the base of said first transistor and its emitter coupled to said predetermined fixed potential, and
- a capacitor (C) coupled between the junction of the bases of said first and second transistor (T_1, T_2) and said predetermined potential.

8. Phase shifter in accordance with at least any one of claims 1 to 6, provided as a differential phase shifter comprising

- a first input (IN+) for inputting an input signal, and
- a second input (IN-) for inputting an inverse input signal,

characterized by at least

- a first transistor with its collector connected to its base and its emitter coupled to a predetermined potential,
- a second transistor with its base connected to the base of said first transistor and its emitter coupled to said predetermined potential,
- a third transistor with its collector connected to its base and its emitter coupled to a predetermined potential,
- a fourth transistor with its base connected to the base of said third transistor and its collector coupled to said predetermined potential, and
- a capacitor (2C) coupled between a first junction of the bases of said first and second transistors and a second junction of the bases of said third and fourth transistors.

9. Phase shifter in accordance with claim 7 or 8, characterized in that said transistors are npn transistors.

10. Phase shifter in accordance with at least any one of claims 7 to 9,

characterized in that said predetermined potential is zero (ground).

11. Data and clock recovery unit comprising a phase detector (20) which includes a phase shifter in accordance with at least any one of the preceding claims.

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